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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,622	08/18/2003	Eugene Feng	2102397-992800	4461

26379 7590 12/02/2005

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EXAMINER	
FAROOQ, MOHAMMAD O	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,622	FENG, EUGENE	
	Examiner	Art Unit	
	Mohammad O. Farooq	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

DOV POPOVICI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morzano et al. U.S. Pat. No. 5,805,931 in view of Pardillos et al. U.S. Pat. No. 5,367,646.

2. As to claim 1, Morzano et al. teach device, comprising:

a decoding circuit for receiving communication signals received via the communication bus, for decoding the communication signals and for generating a plurality of protocol signals in response thereto (item 378, fig.10);

a protocol select circuit for receiving said plurality of protocol signals (i.e. controller circuit; col. 14, lines 8-23).

an array of memory cells (i.e. SAMs; col. 14, lines 8-23); and

said protocol select circuit for configuring the controller circuit in response to the plurality of protocol signals (fig. 7-13; col. 14, lines 8-23).

Morzano et al. do not teach a control circuit for controlling the operation of said array of memory cells. Pardillos et al. teach a control circuit for controlling the operation of said array of memory cells (i.e. memory access controller; col. 21, line 50 – col. 22, line 29). However, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Morzano et al. and Pardillos et al. because that would provide the best use of microprocessor performance wherein it would not be limited by the existence of only one bus (col. 3, line 65 – col. 4, line 7).

3. Claims 2-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morzano et al. U.S. Pat. No. 5,805,931 in view of Pardillos et al. U.S. Pat. No. 5,367,646 further in view of Pereira et al. U.S. Pat. No. 6,542,391 B2.

4. As to claims 2-6, Morzano et al. teach volatile storage element (i.e. DRAM; item 52, fig. 3).

Neither Morzano et al. nor Pardillos et al. teach non-volatile storage element; and volatile storage element is a register, flip-flop, and SRAM. Pereira et al. teach non-volatile storage element; and volatile storage element is a register, flip-flop, and SRAM (col. 18, lines 17-25; col. 9, lines 4-27). However, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the combination of Morzano et al. and Pardillos et al. with Pereira et al. because that would provide memory blocks to store data words having a width determined according to a configuration value (col. 3, lines 3-12).

5. As to claim 7, Morzano et al. teach device comprising:

a decoding circuit for receiving the start field and for generating a plurality of protocol signals (item 378, fig. 10);

a protocol select circuit for receiving said plurality of protocol signals (i.e. controller circuit; col. 14, lines 8-23);

an array of memory cells (i.e. SAMs; col. 14, lines 8-23); and

said protocol select circuit for configuring the controller circuit in response to the plurality of protocol signals (fig. 7-13; col. 14, lines 8-23).

Morzano et al. do not teach a control circuit for controlling the operation of said array of memory cells. Pardillos et al. teach a control circuit for controlling the operation of said array of memory cells (i.e. memory access controller; col. 21, line 50 – col. 22, line 29). However, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Morzano et al. and Pardillos et al. because that would provide the best use of microprocessor performance wherein it would not be limited by the existence of only one bus (col. 3, line 65 – col. 4, line 7).

Neither Morzano et al. nor Pardillos et al. teach non-volatile memory. Pereira et al. teach non-volatile memory (col. 18, lines 17-25). However, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the combination of Morzano et al. and Pardillos et al. with Pereira et al. because that would provide memory blocks to store data words having a width determined according to a configuration value (col. 3, lines 3-12).

6. As to claim 8, neither Morzano et al. nor Pardillos et al. teach protocol select circuit is a flip-flop. Pereira et al. teach protocol select circuit is a flip-flop (col. 18, lines 17-25). However, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the combination of Morzano et al. and Pardillos et al. with Pereira et al. because that would provide memory blocks to store data words having a width determined according to a configuration value (col. 3, lines 3-12).

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morzano et al. U.S. Pat. No. 5,805,931, Pardillos et al. U.S. Pat. No. 5,367,646 and Pereira et al. U.S. Pat. No. 6,542,391 B2 as applied to claims 2-8 above, and further in view of Alexander et al. U.S. Pat. No. 6,188,602 B1.

8. As to claim 9, neither Morzano et al. nor Pardillos et al. or Pereira et al. teach protocol for LPC communication and for FWH communication. Alexander et al. teach protocol for LPC communication (col. 2, lines 53-67) and for FWH communication (col. 3, lines 50 – 61).

However, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the combination of Morzano et al., Pardillos et al. and Pereira et al. with Alexander et al. because that would provide flash memory to be updated during normal operation of the computer system (abstract).

Response to Arguments

9. Applicant's arguments filed August 11, 2005 have been fully considered but they are not persuasive.

The examiner would like to state the rejection is an obviousness rejection not an anticipation rejection. Therefore, the examiner disagrees with the applicant reference Morzano et al. do not teach protocol signal generated by the decoding circuit. Item 378, in figure 11-13, which is a decoder and it generates plurality of signals (decode 0 to decode 3). Furthermore, examiner disagrees with the applicant Morzano et al. fails to show the protocol select circuit which receives the decode signals and configure the controller circuit. This element is taught as the combination of both the Morzano et al. and Pardillos et al. which has been stated above in this final rejection. Finally, as stated earlier in this obviousness rejection, Morzano et al., Pardillos et al. and Pereira et al. teaches various parts of the element containing volatile memory being register, flip-flop, and SRAM and therefore, all of these three references in combination teach the above stated element with volatile memory being register, flip-flop and SRAM.

After considering all of the facts above, the examiner retained the rejection of previously rejected claims.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad O. Farooq whose telephone number is (571) 272-4144. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571) 272-4083. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mohammad O. Farooq
November 14, 2005

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